REMARKS

Applicant submits this amendment responsive to the Office Action dated October 19, 2004, requesting double brackets be used to indicate deletions and an added word in claim 9 be underlined. Applicant has indicated all deletions in the claims with strikethrough notation. The added word in claim 9 has been underlined. For the examiner's convenience, the entire amendment and response is resubmitted herewith.

Claims 1-20 were pending. Claims 21-23 have been added and claims 1, 9 and 17 have been amended. Accordingly, claims 1-23 are pending.

In the present Office Action, the Examiner objected to the language "branch prediction information" in claims 1, 9 and 17. Applicant submits the present amendments overcome the objection. In addition, claims 5 and 13 were also objected. However, Applicant notes Fig. 22 and the related description supports claims 5 and 13. In particular, it is noted that a single L2 cache may include both instructions and branch prediction information.

In the present Office Action, claims 1, 2, 9 and 10 stand rejected under 35 U.S.C. § 102(b), and claims 3-8 and 11-20 stand rejected under 35 U.S.C. § 103(a). Applicant respectfully traverses these rejections.

Claims 1, 2, 9 and 10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Perleberg et al., "Branch Target Buffer Design and Optimization." Applicant submits that each of the pending independent claims are patentable over the cited art. For example, amended claim 1 recites a method including:

> "detecting a first level cache does not contain a first branch prediction information corresponding to a first address;
> determining whether a second level cache contains a second branch prediction information corresponding to said first address, said second branch prediction information comprising a subset of said first branch prediction information;

rebuilding said first branch prediction information in response to determining said second level cache contains said second branch prediction information, wherein said rebuilding comprises:
generating third branch prediction information indicative of a type of branch instruction; and
combining said second branch prediction information with said third branch prediction information;
storing said combined second and third branch prediction information as said first branch prediction information in a first entry of said first level cache, wherein said first entry corresponds to said first address."

Applicant submits at least the above highlighted features of claim 1 are neither taught nor suggested by the cited art. In contrast to the above, Perleberg includes a discussion concerning multilevel BTB's on pages 9-10. This discussion of Perleberg describes each level of a multilevel BTB may include different (e.g, more or less) information. For example, Perleberg teaches "[h]igh performance levels require more storage bits than low performance levels." (page 409, col. 1, para. 2). However, there is no teaching or suggestion in Perleberg of the recited rebuilding of branch prediction information by "generating third branch prediction information indicative of a type of branch instruction; and combining said second branch prediction information with said third branch prediction information" as recited in the claim above. As each of independent claim 9 and 17 include features similar to those of claim 1, each of claims 1, 9 and 17 are believed patentable.

In addition to the above, claims 3, 4, 11, and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perleberg and IBM Technical Disclosure Bulletin, "Partial Address Recording in Branch History Tables" (hereinafter "IBM"). A prima facie case of obviousness of a claimed invention is not established unless all the claim limitations are taught or suggested by the cited prior art. In view of the discussion above, Applicant submits neither Perleberg nor IBM, either singly or in combination, teach or suggest all the features of the recited claims. Accordingly, each of claims 3, 4, 11 and 12 are patentable over the cited art.

In addition, Applicant notes that the Office Action suggests IBM teaches "wherein said branch prediction further comprises information indicating a type of said

branch instruction" which is included in claims 3, 4, 11 and 12. However, in contrast to the recited feature, IBM teaches a special bit may be used to indicate that target instruction address bits are not fully representative of a target address. (IBM, page 3). Accordingly, IBM does not teach the recited information which indicates a "type of said branch instruction."

Applicant also notes that Yung (EP 798632 A2) is cited in the present Office Action with reference to claims 17-20. However, as is the case with Perleberg and IBM, Yung fails to teach the above recited features, either singly or in combination with the other cited art. Accordingly, each of claims 1-20 are patentable in view of Yung as well.

New claims 21-23 are supported by at least Fig. 2 and related description wherein it states: "Fig. 2 shows a portion of one embodiment of branch prediction unit 14. . . . In one embodiment, victim cache 260 is configured to cache only data that was previously held in local predictor storage 206 but was evicted to make room for other data. Advantageously, because local predictor storage 206 and victim cache 260 do not store duplicate data, more branch prediction information may be maintained."

Applicant also notes claims 7 and 15 recite a branch marker bit which may be used in rebuilding a branch prediction. For example, as stated in the description "[u]tilizing the received instructions and branch marker bits, decoder 400 may then rebuild the remaining portion of the branch prediction entry for local predictor storage 206. Decoder may utilize the branch marker bits received via bus 2102 to determine the location of predicted taken branches within the group of instructions received via bus 2104." (page 39). Accordingly, Applicant submits the rejection of claims 7 and 15 is improper.

In any event, Applicant submits each of the independent claims 1, 7 and 19 are patentable over the cited art. Accordingly, each of the dependent claims are patentable as well.

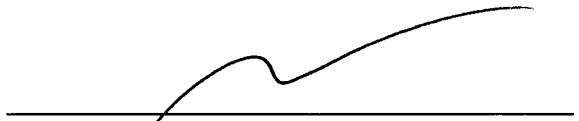
Applicant has also noted the request regarding providing a legend indicating those drawings which represent only prior art. Applicant has considered each of the figures and determined none of the figures represent only prior art. Also, Applicant notes in paragraph 9 of the office action an objection regarding the section headings. However, Applicant is unable to identify any problem with the format of the section headings. If the Examiner believes the objection to be appropriate, Applicant would appreciate specific identification of the matter requiring correction.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-67400/RDR.

Respectfully submitted,



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